IN THE CLAIMS:

Rewrite the pending claims and add new claims as follows:

1. (Cancelled)

2 – 29. (Cancelled)

30. (Currently Amended) An integrated circuit device comprising:

~~an~~ a multiplexor to select data in response to a clock signal, wherein a data bit of the data is selected in response to a transition of the clock signal;

a circuit, coupled to the multiplexor, to regulate a duty cycle of a data signal corresponding to the data in accordance with the clock signal;

a predriver, coupled to the circuit, to adjust a slew rate of the data signal; and

an output driver coupled to the predriver, the output driver including a plurality of transistor stacks to adjust an output drive level of the output driver.

31. (Previously presented) The integrated circuit device of claim 30, wherein the drive level of the output driver is programmable to adjust the output drive level in accordance with a value that is representative of a drive level.

32. (Previously presented) The integrated circuit device of claim 30, wherein a subset of the plurality of transistor stacks are selected to adjust the output drive level of the output driver, wherein the output drive level is based on a predetermined amount of current.

33. (Previously presented) The integrated circuit device of claim 30, wherein a transistor in each transistor stack of the plurality of transistor stacks is binary weighted with respect a transistor in another transistor stack of the plurality of transistor stacks.

34. (Previously presented) The integrated circuit device of claim 30, wherein transistors in the plurality of transistor stacks are sized such that a current drive capability of the output driver is binary weighted.

35. (Previously presented) The integrated circuit device of claim 30, wherein a transistor in each transistor stack of the plurality of transistor stacks has an associated predetermined threshold voltage, and an output voltage from the predriver has a maximum value

corresponding to the predetermined threshold voltage such that the transistor operates in saturation when outputting a predetermined low-level output voltage.

36. (Previously presented) The integrated circuit device of claim 35, wherein the predetermined threshold voltage is substantially between 0.3 and 0.4 Volts.

37. (Previously presented) The integrated circuit device of claim 30, further comprising a voltage generator, coupled to the predriver, to generate a supply voltage for the predriver.

38. (Previously presented) The integrated circuit device of claim 30, wherein the predriver includes a base block and at least one slew rate adjustment block coupled in parallel with the base block, the at least one slew rate adjustment block responsive to a slew rate control signal.

39. (Previously presented) The integrated circuit device of claim 30, further comprising a circuit for increasing a rate at which an output from the predriver transitions from a high-level supply voltage to a low-level supply voltage.

40. (Previously presented) The integrated circuit device of claim 30, wherein the output drive level is such that an output impedance of each transistor stack is maintained within a predetermined range when the transistor stack is outputting a low voltage level.

41. (Previously presented) The integrated circuit device of claim 40, wherein the output impedance substantially exceeds 150 ohms.

42. (Previously presented) The integrated circuit device of claim 30, wherein the predriver distorts the duty cycle of the data signal by a predetermined amount and the circuit to regulate the duty cycle modifies the duty cycle of the data signal such that data output using the output driver is substantially symmetric.

43. (Previously presented) The integrated circuit device of claim 30, wherein the circuit to regulate the duty cycle includes at least one stacked transistor pair that is controlled by a control bit such that, when the control bit is enabled, the data signal transitions from a high level to a low level earlier than transitions in the clock signal.

44. (Previously presented) The integrated circuit device of claim 30, further comprising:

a charge compensation circuit to provide an amount of charge to a supply voltage for the predriver in accordance with a charge compensation value; and

a charge compensation value generator, coupled to the charge compensation circuit, the charge compensation value generator including:

a voltage generator;

a test circuit; and

a logic circuit;

wherein the charge compensation value generator is configured to determine the charge compensation value using the logic circuit in accordance with a current at an output of the voltage generator when the voltage generator supplies a voltage to the test circuit.

45. (Previously presented) The integrated circuit of claim 44, wherein the charge compensation value is determined such that the current at the output of the voltage generator is substantially zero.

46. (Previously presented) The integrated circuit of claim 44, wherein the test circuit provides a model of charge consumption characteristics of a circuit in the integrated circuit device.

47. (Previously presented) The integrated circuit of claim 44, wherein the charge compensation value is determined iteratively.

48. (Previously presented) An integrated circuit device comprising:

means for selecting data in response to a clock signal, wherein a data bit of the data is selected in response to a transition of the clock signal;

means for regulating a duty cycle of a data signal corresponding to the data in accordance with the clock signal;

means for adjusting a slew rate of the data signal; and

means for adjusting an output drive level of the data signal.

49. (Currently Amended) An integrated circuit device comprising:

~~an~~ <u>a</u> multiplexor to select data in response to a clock signal, wherein a data bit of the data is selected in response to a transition of the clock signal;

a predriver, coupled to the ~~circuit~~ <u>multiplexor</u>, to adjust a slew rate of [[the]] <u>a</u> data signal <u>output by the multiplexor</u>;

a voltage generator, coupled to the predriver, to generate a supply voltage for the predriver; and

an output driver coupled to the predriver, the output driver including a plurality of transistor stacks <u>connected in parallel to a data signal output of the output driver</u> to adjust an output drive level of the output driver.

50. (Previously presented) The integrated circuit device of claim 49, wherein the drive level of the output driver is programmable to adjust the output drive level in accordance with a value that is representative of a drive level.

51. (Previously presented) The integrated circuit device of claim 49, wherein a subset of the plurality of transistor stacks are selected to adjust the output drive level of the output driver, wherein the output drive level is based on a predetermined amount of current.

52. (Previously presented) The integrated circuit device of claim 49, wherein a transistor in each transistor stack of the plurality of transistor stacks is binary weighted with respect a transistor in another transistor stack of the plurality of transistor stacks.

53. (Previously presented) The integrated circuit device of claim 49, wherein transistors in the plurality of transistor stacks are sized such that a current drive capability of the output driver is binary weighted.

54. (Previously presented) The integrated circuit device of claim 49, wherein a transistor in each transistor stack of the plurality of transistor stacks has an associated predetermined threshold voltage, and an output voltage from the predriver has a maximum value corresponding to the predetermined threshold voltage such that the transistor operates in saturation when outputting a predetermined low-level output voltage.

55. (Previously presented) The integrated circuit device of claim 54, wherein the predetermined threshold voltage is substantially between 0.3 and 0.4 Volts.

56. (Previously presented) The integrated circuit device of claim 49, wherein the predriver includes a base block and at least one slew rate adjustment block coupled in parallel with the base block, the at least one slew rate adjustment block responsive to a slew rate control signal.

57. (Previously presented) The integrated circuit device of claim 49, further comprising a circuit for increasing a rate at which an output from the predriver transitions from a high-level supply voltage to a low-level supply voltage.

58. (Previously presented) The integrated circuit device of claim 49, wherein the output drive level is such that an output impedance of each transistor stack is maintained within a predetermined range when the transistor stack is outputting a low voltage level.

59. (Previously presented) The integrated circuit device of claim 58, wherein the output impedance substantially exceeds 150 ohms.

60. (Previously presented) The integrated circuit device of claim 49, further comprising:

a charge compensation circuit to provide an amount of charge to a supply voltage for the predriver in accordance with a charge compensation value; and

a charge compensation value generator, coupled to the charge compensation circuit, the charge compensation value generator including:

a voltage generator;

a test circuit; and

a logic circuit;

wherein the charge compensation value generator is configured to determine the charge compensation value using the logic circuit in accordance with a current at an output of the voltage generator when the voltage generator supplies a voltage to the test circuit.

61. (Previously presented) The integrated circuit of claim 60, wherein the charge compensation value is determined such that the current at the output of the voltage generator is substantially zero.

62. (Previously presented) The integrated circuit of claim 60, wherein the test circuit provides a model of charge consumption characteristics of a circuit in the integrated circuit device.

63. (Previously presented) The integrated circuit of claim 60, wherein the charge compensation value is determined iteratively.

64. (Currently Amended) An integrated circuit device comprising:

~~an~~ a multiplexor to select data in response to a clock signal, wherein a data bit of the data is selected in response to a transition of the clock signal;

a predriver, coupled to the ~~circuit~~ multiplexor, to adjust a slew rate of [[the]] a data signal output by the multiplexor;

a charge compensation circuit to provide an amount of charge to a supply voltage for the predriver in accordance with a charge compensation value; and

an output driver coupled to the predriver, the output driver including a plurality of transistor stacks connected in parallel to a data signal output of the output driver to adjust an output drive level of the output driver.

65. (Previously presented) The integrated circuit device of claim 64, wherein the drive level of the output driver is programmable to adjust the output drive level in accordance with a value that is representative of a drive level.

66. (Previously presented) The integrated circuit device of claim 64, wherein a subset of the plurality of transistor stacks are selected to adjust the output drive level of the output driver, wherein the output drive level is based on a predetermined amount of current.

67. (Previously presented) The integrated circuit device of claim 64, wherein a transistor in each transistor stack of the plurality of transistor stacks is binary weighted with respect a transistor in another transistor stack of the plurality of transistor stacks.

68. (Previously presented) The integrated circuit device of claim 64, wherein transistors in the plurality of transistor stacks are sized such that a current drive capability of the output driver is binary weighted.

69. (Previously presented) The integrated circuit device of claim 64, wherein a transistor in each transistor stack of the plurality of transistor stacks has an associated predetermined threshold voltage, and an output voltage from the predriver has a maximum value corresponding to the predetermined threshold voltage such that the transistor operates in saturation when outputting a predetermined low-level output voltage.

70. (Previously presented) The integrated circuit device of claim 69, wherein the predetermined threshold voltage is substantially between 0.3 and 0.4 Volts.

71. (Previously presented) The integrated circuit device of claim 69, further comprising a voltage generator, coupled to the predriver, to generate a supply voltage for the predriver.

72. (Previously presented) The integrated circuit device of claim 69, wherein the predriver includes a base block and at least one slew rate adjustment block coupled in parallel with the base block, the at least one slew rate adjustment block responsive to a slew rate control signal.

73. (Previously presented) The integrated circuit device of claim 69, further comprising a circuit for increasing a rate at which an output from the predriver transitions from a high-level supply voltage to a low-level supply voltage.

74. (Previously presented) The integrated circuit device of claim 69, wherein the output drive level is such that an output impedance of each transistor stack is maintained within a predetermined range when the transistor stack is outputting a low voltage level.

75. (Previously presented) The integrated circuit device of claim 74, wherein the output impedance substantially exceeds 150 ohms.

76. (Previously presented) The integrated circuit device of claim 69, further comprising:

a charge compensation value generator, coupled to the charge compensation circuit, the charge compensation value generator including:

a voltage generator;

a test circuit; and

a logic circuit;

wherein the charge compensation value generator is configured to determine the charge compensation value using the logic circuit in accordance with a current at an output of the voltage generator when the voltage generator supplies a voltage to the test circuit.

77. (Previously presented) The integrated circuit of claim 76, wherein the charge compensation value is determined such that the current at the output of the voltage generator is substantially zero.

78. (Previously presented) The integrated circuit of claim 76, wherein the test circuit provides a model of charge consumption characteristics of a circuit in the integrated circuit device.

79. (Previously presented) The integrated circuit of claim 76, wherein the charge compensation value is determined iteratively.